2815

PATENT
0941-0316P

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant: Ming-Dou KER et al. Conf.: 9842

Appl. No.: 09/944,171 Group: 2815

Filed: September 4, 2001 Examiner: J.A. FENTY

For: ESD PROTECTION CIRCUIT WTH VERY LOW INPUT CAPACITANCE FOR HIGH-FREQUENCY I/O PARTS

LARGE ENTITY TRANSMITTAL FORM

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

May 12, 2003

Sir:

Transmitted herewith is an amendment in the above-identified application.

☐ The enclosed document is being transmitted via the Certificate of Mailing provisions of 37 C.F.R. § 1.8.

☐ The enclosed document is being transmitted via facsimile.

The fee has been calculated as shown below:

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA	RATE	ADDITIONAL FEE
TOTAL	17	-	20	=	0	$ 18	$0.00
INDEPENDENT	1	-	3	=	0	$ 84	$0.00
☐ FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM						$280	$0.00
						TOTAL	$0.00

☐ Petition for ( ) month(s) extension of time pursuant to 37 C.F.R. §§ 1.17 and 1.136(a). $0.00 for the extension of time.

☒ No fee is required.

☐ Check(s) in the amount of $0.00 is(are) enclosed.

☐ Please charge Deposit Account No. 02-2448 in the amount of $0.00. This form is submitted in triplicate.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By _____
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KM/RFG/ndb
0941-0316P

Attachment(s)

(Rev. 04/30/03)

#7A Amdt. SDavis 5/21/03

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For: ESD PROTECTION CIRCUIT WTH VERY LOW INPUT CAPACITANCE FOR HIGH-FREQUENCY I/O PARTS

AMENDMENT UNDER 37 C.F.R. § 1.111

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

May 12, 2003

Sir:

In response to the Examiner's Office Action dated February 12, 2003, the following amendments and remarks are respectfully submitted in connection with the above-identified application.

IN THE CLAIMS:

Please rewrite claims 7, 8, 13 and 15 as follows:

7. (Amended) The ESD protection circuit as claimed in claim 6, wherein the substrate-triggered MOS includes a gate applied with a bias voltage to keep the substrate-triggered MOS off during normal operations.